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| EXAMINER | |
|---|---|
| SHAH, TUSHAR S | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2184 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/552,778 | GANGWAL, OM PRAKASH | |
| | Examiner | Art Unit | |
| | TUSHAR S. SHAH | 2184 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *15 January 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1 and 3-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

**DETAILED ACTION**

This action is in response to the amendment filed on January 15th, 2009.

***Status of Claims***

Claims 1 and 3-13 are pending, of which claims 1, 8, 9, 12 and 13 are in independent form.

***Response to Arguments***

1. Applicant's arguments filed on 1/15/2009 have been fully considered but they are not persuasive.

**Regarding claim 1**, applicant has argued, on pages 12-13 of the response, that the cited Nadehara reference does not disclose an Application Program Interface that operates the circular buffer and suggests that Nadehara is only directed to an internal implementation of a circular buffer.

Referring to applicant's arguments to claim 1, the system disclosed in Nadehara is controlled by software stored in the program memory (See column 2, lines 36-41).

**Also regarding claim 1**, applicant has argued, on pages 13-14 of the response, that Nadehara fails to disclose returning a pointer because Nadehara is only an internal implementation.

Referring to applicant's second argument to claim 1, as established above, Nadehara is operated by a software program. Further, Nadehara provides an index value which is altered based upon whether or not a wrap around occurs. If there is no wrap around the index is used to determine the appropriate address and if there is a wrap around the index is altered to ensure an in range address is provided (See Fig. 7 steps 108-110).

**Regarding claim 4**, the applicant has argued, one page 15 of the response, that paragraph 0005 does not admit prior art.

As per applicant's arguments to claim 4, the cited section refers to the use of different grain sizes as typical, which is taken to mean well known in the art and further the process is also described in the NPL document (dated 2002) provided by the applicant in the IDS dated 10/12/2005. It is seen by the examiner as a process well known in the prior art.

**Regarding claims 4 and 11**, the applicant has argued, on page 15 of the response, that the claims are allowable for at least the same reasons as independent claim 1.

As per applicant's arguments to claims 4 and 11, as the issues with claim 1 have been resolved in the above arguments, the rejections to these claims are maintained.

The grounds of rejection to claims 1 and 3-13 are maintained and repeated below. The rejections have been updated to reflect the claim amendments made.

***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3, 5-10, 12 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Nadehara US Patent No. 5,535,412 (hereinafter Nadehara).

**Referring to claim 1**, Nadehara discloses, a data processing apparatus, comprising a processing circuit (circular buffer controller in Fig. 6) arranged to execute a data producing

process (external input register 12 for keeping a new value to be fed to the circular buffer, column 3, lines 54-56) and a data consuming process (index register 2 indicates the current object of operation, column 3, lines 36-37), the data producing process producing a stream of data ( data being input into external input register 12, Fig. 6) and the data consuming process consuming the stream of data concurrently with production of the stream (data is read out of data memory 4, column 4, lines 23-26);

Processing memory accessible to the data consuming process (program memory 17, Fig. 6);

A first-in first-out circular buffer unit (the circular buffer 33 is contained in data memory 4, column 4, lines 9-12) for passing data from the stream between the data producing process and the data consuming process, the circular buffer unit comprising buffer memory (data memory 4, Fig. 6) and writing data-items from the stream in a circular fashion into the buffer memory (the circular buffer area is an N element circular buffer, column 4, lines 10-14); and

A consuming process application program interface (API) of the circular buffer unit (software stored in the program memory, column 2, lines 36-41), the consuming process API being arranged to:

Access an auxiliary memory region accessible to the data consuming process (in order to deal with a wrap around condition a copy of the circular buffer is provided after the circular buffer area in memory, column 1, lines 60-64),

process a command for making a data grain from the stream available to the data consuming process (data from the circular buffer area is stored in data register 5 to have an arithmetic operation may be performed on it, column 5, lines 35-38),

Respond to the command by testing whether addresses of data within the grain to which access has to be gained wrap around in the buffer memory (the value of the block length register 10 is added to that of the index register 2, and the result is compared with the element number register 7 and if the value is greater than or equal to the value N, column 4, lines 52-60),

Copy, in response to detection that the addresses wrap around, the grain from the buffer memory to the auxiliary memory region, so that the wrap around is eliminated in the copied grain (in the event that an arithmetic operation is achieved beyond a circular buffer area, a copy of the circular buffer area is provided after the circular buffer area, column 1, lines 60-64), and

return a pointer to the consuming process indicating a location in the buffer memory from which to read the entire

grain when the addresses do not wrap around inside the grain, or a pointer indicating a location of the auxiliary memory region from which to read the entire grain when the addresses wrap around (The value of the block length register is added to the index register to move the operation through the circular buffer and if the value of the resulting value of the index is greater than the element number register, the value of the element number is subtracted from the index and the operation occurs with the values in the wrap around portion of memory otherwise the operations are carried out on the data in the range of the circular buffer area, Figs. 7 and 9).

**As per claim 3**, Nadehara discloses, the consuming process is arranged to select an address of the auxiliary memory and a grain size as part of the command (Step 106, Fig. 7).

**As per claim 5**, Nadehara discloses, the data producing process is arranged to use variable grain sizes for sending data (the block length register specifies the size of data to be processed at a time and it is seen as inherent that it may change, column 3, lines 51-52).

**As per claim 6**, Nadehara discloses, a first grain size and a size of the circular buffer unit are selected so that addresses of the data in the circular buffer unit always wrap around between successive grains of the first grain size (It is identified by Nadehara that this is the standard operation of prior art systems, column 1, lines 53-57 and Fig 5).

**As per claim 7**, Nadehara discloses, containing a further processing memory (circular buffer controller in Fig. 6) accessible to the data producing process (external input register 12 for keeping a new value to be fed to the circular buffer, column 3, lines 54-56) for producing the data stream;

A producing process application program interface (API) (External input register, Fig. 6) of the circular buffer unit, arranged to:

receive a further auxiliary memory region selection for the data producing process (in order to deal with a wrap around condition a copy of the circular buffer is provided after the circular buffer area in memory, column 1, lines 60-64),

process a further command for outputting an output data grain from the stream (data from the circular buffer area is stored in data register 5 to have an arithmetic operation may be performed on it, column 5, lines 35-38),

respond to the further command by testing whether addresses of data within the output grain will wrap around in the buffer memory step 123, Fig. 8);

return a pointer indicating a location in the buffer memory to which the producing process writes the entire grain when the addresses do not wrap around inside the grain, or a pointer indicating a location of the further auxiliary memory region to which the producing process writes the entire grain, when the addresses wrap around (if the value of the input index register is greater than the value of the block length register, the value of the element number register is added to the write address to generate the replica addresses past the circular buffer area, Fig. 8), and

Copy, in response to detection that the addresses wrap around, the entire grain from the further auxiliary memory region to the buffer memory so that the wrap around is created in the copied grain (the values from the external input register are written into the replica addresses in a wrap around, Fig. 8).

**Referring to claim 8**, Nadehara discloses, a data processing apparatus, comprising: a processing circuit (circular buffer controller in Fig. 6), arranged to execute a data producing

process (external input register 12 for keeping a new value to be fed to the circular buffer, column 3, lines 54-56) and a data consuming process (index register 2 indicates the current object of operation, column 3, lines 36-37), the data producing process producing a stream of data ( data being input into external input register 12, Fig. 6), the data consuming process consuming the stream of data concurrently with production of the stream (data is read out of data memory 4, column 4, lines 23-26);

Processing memory accessible to the data producing process (program memory 17, Fig. 6);

A first-in first-out circular buffer unit (the circular buffer 33 is contained in data memory 4, column 4, lines 9-12) for passing data from the stream between the data producing process and the data consuming process, the circular buffer unit comprising buffer memory (data memory 4, Fig. 6), writing data-items from the stream in a circular fashion into the buffer memory (the circular buffer area is an N element circular buffer, column 4, lines 10-14); and

A producing process application program interface (API) of the circular buffer unit (External input register, Fig. 6), the producing process API being arranged to:

access an auxiliary memory region accessible to the data producing process (in order to deal with a wrap around condition

a copy of the circular buffer is provided after the circular buffer area in memory, column 1, lines 60-64),

process a command for making memory available to the data producing process for writing a produced grain (Steps 121 and 122 in Fig. 8),

respond to the command by testing whether addresses of data within the grain for which memory has to be made available wrap around in the circular buffer memory (Step 123 in Fig. 8), and

return a pointer to the producing process indicating a location in the buffer memory to which to write the entire grain when the addresses do not wrap around inside the grain, or a pointer indicating a location of the auxiliary memory region to which to write the entire grain, when the addresses wrap around (Steps 124 and 125 in Fig. 8).

**Referring to claim 9**, Nadehara discloses, a machine implemented method for implementation of a signal processing task (data is read out of data memory 4, column 4, lines 23-26), comprising, concurrently executing processes between which a data stream is communicated via a circular buffer memory (circular buffer controller in Fig. 6), the method comprising:

Providing an application program interface (API) that provides for selectable definition of grain size and an

auxiliary memory region (Step 106, Fig. 7), the API including a function to be called by a data consuming one of the processes to gain access to a grain of data stored in the buffer memory (data is read out of data memory 4, column 4, lines 23-26) wherein the function is arranged to:

test whether addresses of the grain to which access has to be gained wrap around in the buffer memory (Step 109, Fig. 7),

copy the entire grain from the buffer memory to the auxiliary memory region when the addresses wrap around in the grain, so that the wrap around is eliminated in the copied grain, and

return, as a result of the call, a pointer to the consuming one of the processes indicating a location in buffer memory from which to read the entire grain when the addresses do not wrap around inside the grain, or a pointer indicating the location of the auxiliary memory from which to read the entire grain, when the addresses wrap around in the grain (The value of the block length register is added to the index register to move the operation through the circular buffer and if the value of the resulting value of the index is greater than the element number register, the value of the element number is subtracted from the index and the operation occurs with the values in the wrap around portion of memory otherwise the operations are carried

out on the data in the range of the circular buffer area, Figs. 7 and 9);

Receiving a specification of the signal processing task; identifying a call to said function in the specification of the signal processing task (program memory 17 stores software to control the operation of the system, column 3-4, lines 67 and 1-2);

implementing the call using the function from the API (the instruction execution controller controls operations by referencing the program memory and comparators, column 4, lines 1-5).

**As per claim 10**, Nadehara discloses, the API hides a distribution of processes over processing elements from the specification of the processing task, the implementation of the function being selected according to the distribution (the instruction execution controller 18, controls reading from the circular buffer by referencing the program memory and data from comparators, column 4, lines 1-5).

**Referring to claim 12**, corresponding limitations as presented in claim 1 are recited. Therefore the rejection of claim 1 applies to claim 12.

**Referring to claim 13,** corresponding limitations as presented in claim 8 are recited. Therefore the rejection of claim 8 applies to claim 13.

***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nadehara US Patent No. 5,535,412 (hereinafter Nadehara) as applied to claims 1 above, and further in view of Applicant's Admitted Prior Art (hereinafter AAPA).

**As per claim 4,** Nadehara does not appear to explicitly disclose, the data producing process and the data consuming process are arranged to use a first and second grain size for sending data to and receiving data from the circular buffer unit

respectively, the first and second grain size differing from one another.

However, the Applicant has admitted this as solved in the prior art (AAPA specification page 1, lines 25-30).

The suggestion/motivation would have been that it would be clear to one of ordinary skill that there are many applications where the output portions of a system may be fixed to a certain size, yet data may be received in a different size.

3. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nadehara US Patent No. 5,535,412 (hereinafter Nadehara) as applied to claim 10 above, further in view of Sample et al. US Patent No. 5,477,475 (hereinafter Sample)

**As per claim 11**, it is noted that Nadehara does not appear to explicitly disclose, generating integrated circuit manufacturing control information for implementing the machine implementation, and manufacturing an integrated circuit under control of the integrated circuit manufacturing control information.

However, Sample discloses, generating integrated circuit manufacturing control information for implementing the machine implementation, and manufacturing an integrated circuit under

control of the integrated circuit manufacturing control information (a system for integrated design where a hardware prototype is generated by a user's schematics and the prototype is electrically reconfigurable and maybe updated without changing the wiring, column 2, lines 13-20).

At the time of the invention, it would have been obvious to one of ordinary skill in the art having the teachings of Nadehara and Sample before him or her to implement the system of Nadehara on a programmable device as in Sample.

The suggestion/motivation for doing so would have been that building the system of Nadehara on an FPGA is a low cost option that would allow for updating and testing of multiple embodiments without building many prototypes. FPGA's maybe programmed to build a circuit and then reset to the build another without significant delay.

Therefore it would have been obvious to combine Sample with Nadehara to obtain the invention as specified in the instant claims

***Conclusion***

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

***Contact Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TUSHAR S. SHAH whose telephone number is (571)270-1970. The examiner can normally be reached on Mon-Fri 7:30am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dr. Henry Tsai can be reached on 571-272-4176. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/T. S. S./
Examiner, Art Unit 2184

**/Henry W.H. Tsai/**
**Supervisory Patent Examiner, Art Unit 2184**